

The BTeV Pixel Readout Chip

David Christian

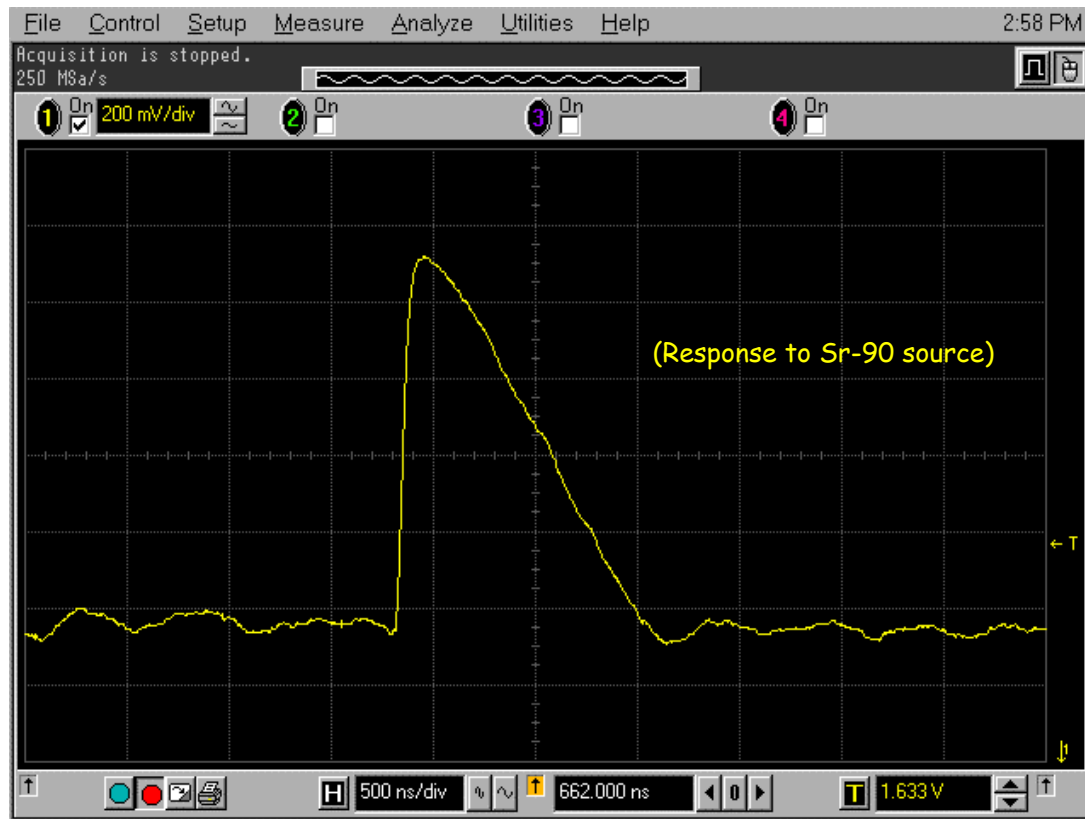
- Radiation hard.
- Able to tolerate large sensor leakage current.
- Optimized for use at the Tevatron Collider.
- Very high speed zero-suppressed readout.
 - Lowest level trigger is pixel based → all data from every crossing must be read out.
 - Spectrometer design luminosity = 15 MHz interaction rate.
 - Pixel readout chip requirement = minimal data loss at 45 MHz interaction rate.

- FPIX0 (0.8 μ CMOS)
 - Fully functional pixel chip (low speed readout).
 - Used with ATLAS prototype sensors.
 - Proved value of low resolution pulse height measurement.
- FPIX1 (0.5 μ CMOS)
 - High speed readout (not high enough).
- FPIX2 (0.25 μ CMOS)
 - Very high speed readout (meets requirement).
 - Radiation hard.
- One more iteration required.
 - Need to integrate a test pulser.

- 0.25 μ CMOS design started in 1998; verified in a series of small test chips.
 - Tested to 87 Mrad with no degradation in analog performance and only minor changes required to bias conditions.
 - Digital cells insensitive to total dose.
 - No latch-up, no gate rupture.
 - Single event upset cross sections measured, typically less than 10^{-15} cm⁻² per bit.
 - Measured with 200 MeV protons; about the same for MIP's.
 - Expected upset rates: ~10 pixel kill bits/hr, 2 DAC register bits/hr, 1 data serializer bit/hr.
 - Will reload kill pattern each fill, & monitor other registers & reset as necessary (can be done without interrupting data taking for most errors).

Leakage Current Compensation

- Pulse response of cell (0,0) with $\sim 55\text{nA}$ per pixel sensor leakage current.
 - Tesla p-spray sensor/FPIX2A hybrid (VTT solder bumps).
 - Data taken at room temperature 1 week after $7\text{E}13\text{cm}^{-2}$ (protons).
 - Sensor bias = 250V , $I_{\text{leak}} = 108\mu\text{A}$ for single-chip sensor.



- Timewalk is *much* less of a problem than at the LHC.
- Can minimize (FE noise \otimes Disc. threshold dispersion) without trim DAC's in every pixel.
 - Allows low discrimination levels ($<3000 e^-$)

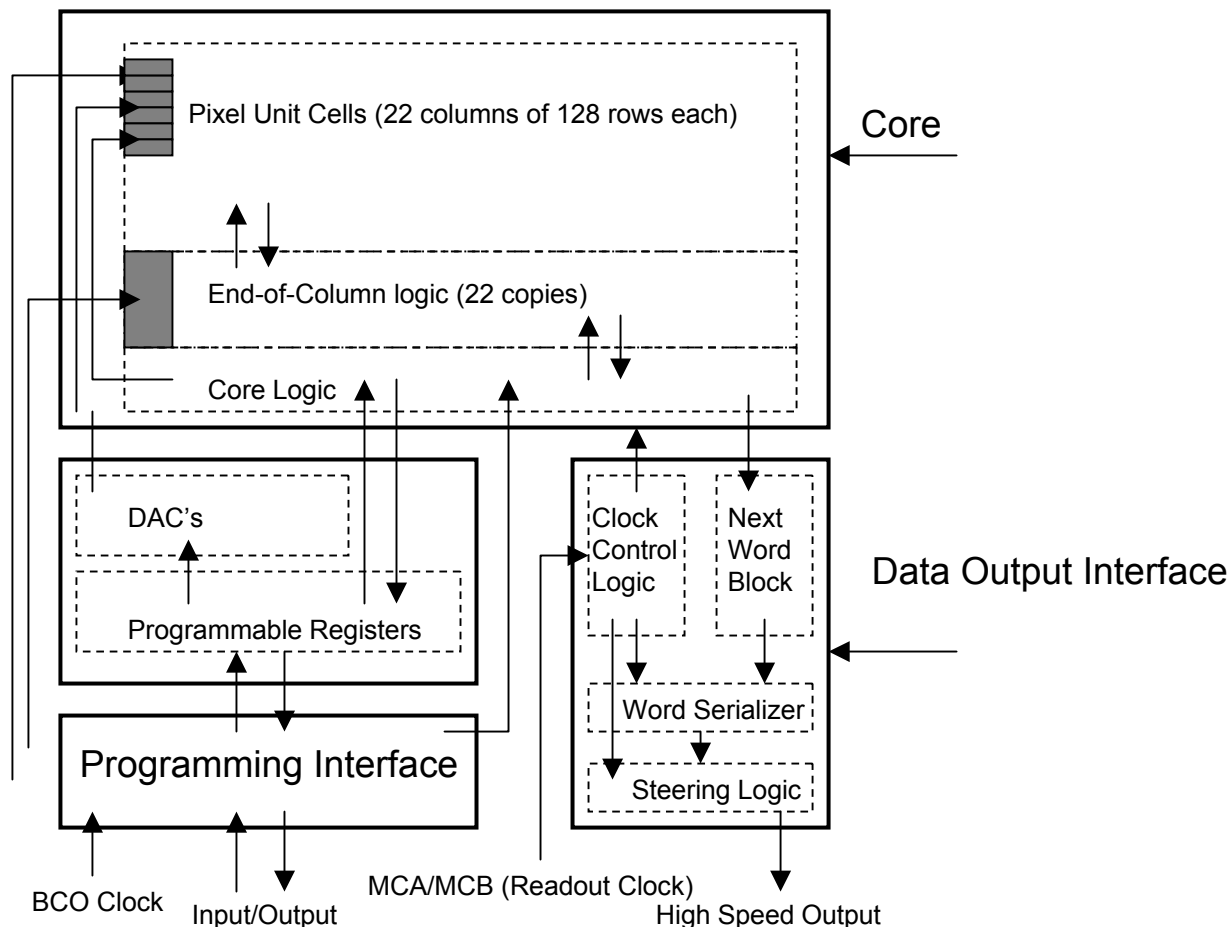
- Data kept in pixels until it is serialized and transmitted off chip – no buffer memory.
- Occupancy varies more than a factor of ten from the corner of the detector closest to the beam to the corners furthest from the beam → Flexible serial data output interface allows the use of 1, 2, 4, or 6 output links (each 140 Mbps).

FPIX2 Block Diagram

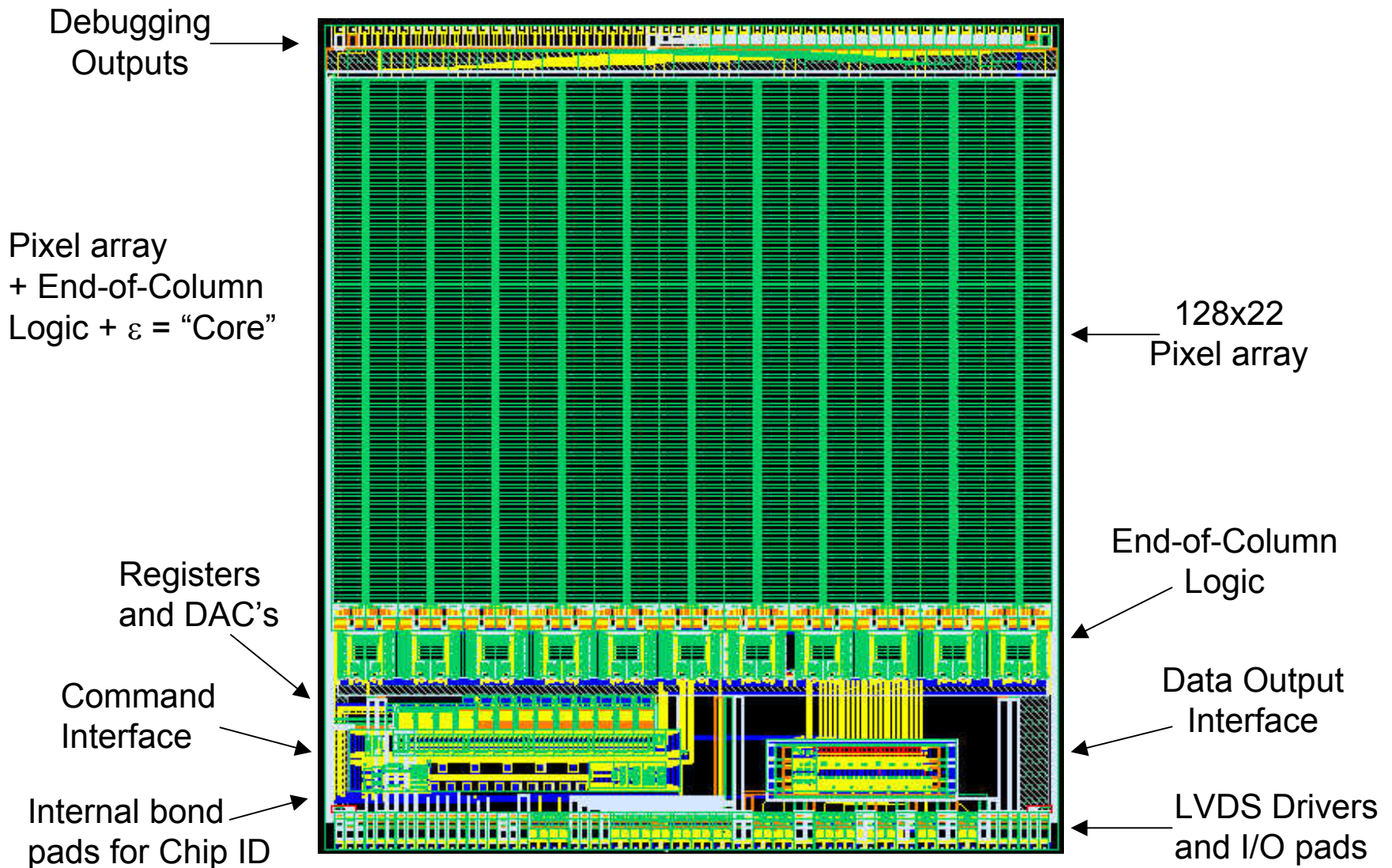
Fabricated by TSMC
(through MOSIS).
Received early 2003.

Only bias voltages
required are 2.5V &
ground.

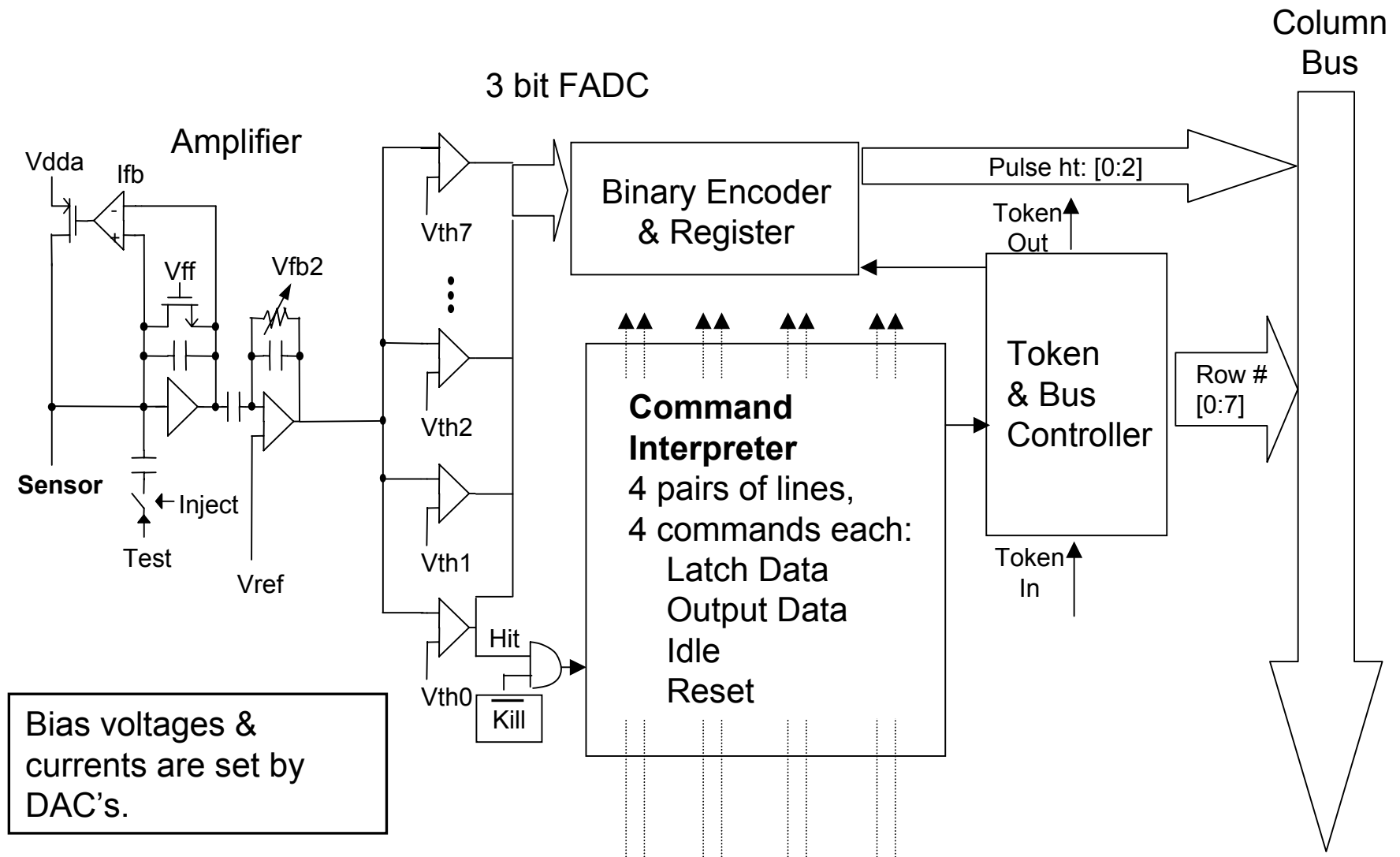
All I/O is LVDS.



FPIX2 Layout

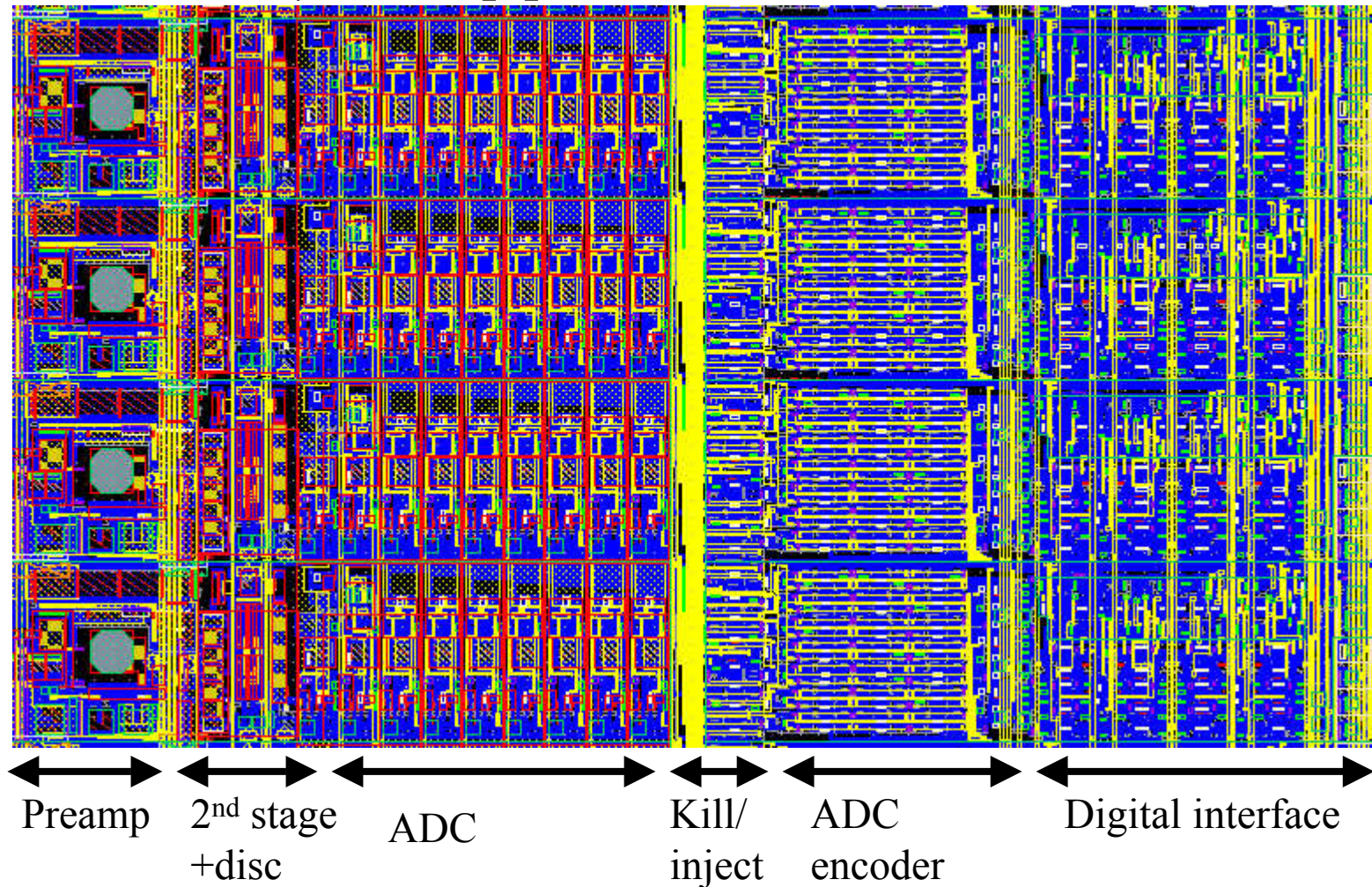


Pixel Unit Cell



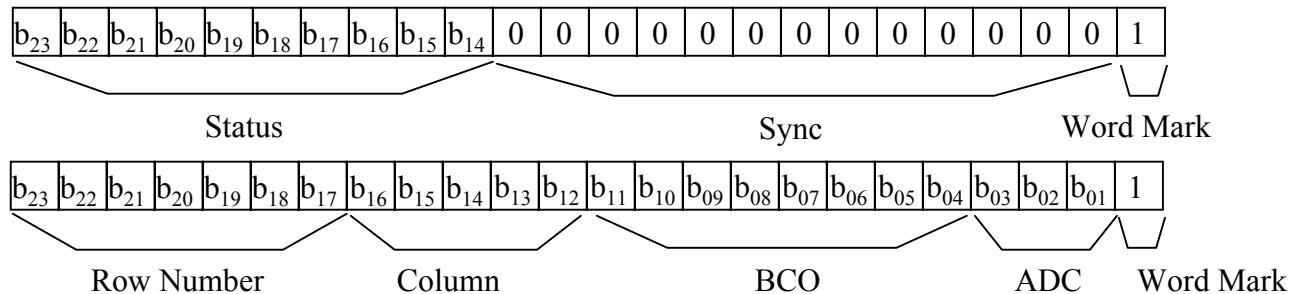
$BTeV$
 C_0 Pixel Cells (four 50 x 400 mm cells)

12 μ m bump pads



- Data is driven off of a hit pixel onto the Core output bus, which is 23 bits wide. The data word consists of the information generated in the pixel unit cell (7 bit row number, and 3 bit ADC value), plus a 5 bit column number and an 8 bit BCO number, which are added by the end of column logic.
- The Data Output Interface latches data from the Core output bus on the *falling* edge of the readout clock, serializes the data, and drives it off chip.

Output Data Format



- Five bits are used to encode 22 columns. The column numbering scheme has no column number ending in 00. This ensures that a data word can never have 0's in b₀₁ – b₁₃. This feature distinguishes a data word from a sync/status word.
- Synchronization between the FPIX2 and the Pixel Data Combiner Board is established and maintained using the “sync/status” word. Whenever no data is available for output, the FPIX2 transmits the sync/status word. At least two sync/status words are guaranteed to be output every time the column number decreases. In addition, 23 bit hit data is transferred using a 24 bit word. The PDCB uses the word mark bit as a sync check on every word transfer.

RCLK and SCLK

- The core readout clock (RCLK) is derived from the serial clock (SCLK). SCLK is constructed from external clocks and is nominally 140 MHz.
- The frequency of RCLK depends on the number of output pairs being used. This relationship means that no buffer memory is required in the Data Output Interface.

Configuration	SCLK Frequency	RCLK Frequency	
6 output pairs	140 MHz	35 MHz	140(6/24)
4 output pairs	140 MHz	23.3 MHz	140(4/24)
2 output pairs	140 MHz	11.7 MHz	140(2/24)
1 output pair	140 MHz	5.8 MHz	140(1/24)

- Designers are currently finishing FSSR (silicon strip readout chip) modifications.
- FSSR & FPIX share digital logic → very little additional design work required for FPIX.
 - FPIX pulser will be slightly different than FSSR pulser (polarity, offset, & “triangle” vs. square).
- Expect submission in Spring '05.